A Silicon-on-Insulator 28-V RF Power LDMOSFET for 1-GHz Integrated Power Amplifier Applications

Erik McShane, Krishna Shenai, and S. K. Leong[+]
MicroSystems Research Center, University of Illinois at Chicago, Chicago, IL, 60607, USA
[+]PolyFET RF Devices, Camarillo, CA, 93012

***Abstract*—This paper presents the first results of a 1-GHz SOI RF power LDMOSFET with 115 mW of output power. A 6-W P_{OUT} (competitive with comparable bulk LDMOSTs) can be achieved by scaling the FET dimensions with little degradation of RF performance. Both DC and RF characteristics are presented, and model parameters are extracted. Class A amplifier results are shown to deliver a PAE of 25%, power gain of 16 dB, and 1-dB compression of 40 mW. These results are extremely encouraging for IPA development with SOI RF power LDMOSFETs.**

I. Introduction

Power amplifiers for wireless applications are evolving into monolithic implementations (e.g. integrated power amplifiers, IPAs). This trend is motivated by demands for compact, low cost, and efficient RF front ends in commercial and military sectors. Presently GaAs MESFETs [1]-[4] and SiGE HBTs [5]-[6] are more viable than vanilla Si. The semi-insulating GaAs substrate permits high-Q passives for on-chip matching; SiGe has poorer passives but higher power gain and power density.

Silicon LDMOSFETs have many attractive properties for including high PAE and co-fabrication with signal-level devices. However, the lossy substrate prevents the integration of the high-*Q* passives, particularly inductors, which are needed for tuning and matching. The buried dielectric of SOI LDMOSFETs, though, permits high-*Q* (> 10) passives and prevents inter-device noise due to the elimination of substrate coupling currents [7]-[8]. SOI also exhibits better thermal performance than bulk devices.

This paper presents results of 28-V RF SOI power LDMOSFETs fabricated using a modified 1.2-µm SOI CMOS process. Room temperature measurements were performed, and the DC characteristics were used to extract parameters for a bulk LDMOSFET circuit simulation model. Then RF characteristics were obtained and used to optimally bias the device. Finally, a class A amplifier was constructed, and input/output matching was performed to obtain maximum power output. Initial results of the SOI LDMOSFET are very encouraging. With further optimization we expect this device to be competitive with state-of-the-art GaAs MESFET and SiGe HBT performance, leading to strong prospects for IPAs based on SOI RF power LDMOSFETs.

This paper is arranged in several sections. First the device fabrication is described. Then DC and RF results of the LDMOST are presented. Next, model parameters are extracted from the measured data. Finally, results are shown of a class A amplifier constructed with this device.

II. Device Fabrication

The fabrication process was modified from a 1.2-µm SOI CMOS line to include the *p*-body implant. Also, an elongated lightly-doped drain (LDD) feature was formed to provide the high blocking voltage (>35 V) necessary in this device. The high blocking voltage is required since the device is intended for operation at a 7.5-V DC bias, and inductor kickback may result in voltage transients of three times the DC bias. The structure is shown in Fig. 1.

Beginning with a 0.2-µm *p*-type SIMOX substrate having a resistivity of 3,000 Ω-cm, a 0.14-µm *p*-type epitaxial layer (1×10^{15} cm^{-3}) was grown. Then a 500-Å gate oxide was grown. A 0.4-µm polysilicon gate was then deposited and doped with phosphorus (3×10^{15} cm^{2}, 80 KeV). Then a boron implantation (3×10^{12} cm^{2}, 90 KeV) at a 45° slant was performed for V_T adjustment. The angle implantation energy and slant were optimized using numerical simulation (ATHENA) to produce a penetration under the gate of approximately 0.6 µm. After the V_T adjust, the LDD was formed by a blanket implant of arsenic (2×10^{12} cm^{2}, 80 KeV). The gate-to-drain overlap was also optimized to be 0.1 µm.

The source n^+ implant was self aligned to the gate spacer, but the drain n^+ implant was offset from the gate to preserve the LDD. To provide the biasing of the body region an interleaved finger arrangement was used in which narrow p^+ implants were inserted into the typical n^+ source implant. Then the source and drain regions were formed using a two-step implantation of phosphorus and arsenic (each at 2×10^{14} cm^{2}, 85 KeV). To produce a dense cell layout, explicit contact openings to the body ties were removed; instead the electrical short between the source and body was obtained by self-aligned silicidation (CoSi) of the source.

After fabrication, devices were also packaged in a leaded RF package consisting of a quarter-inch square ceramic-based carrier mounted on a copper-tungsten flange.

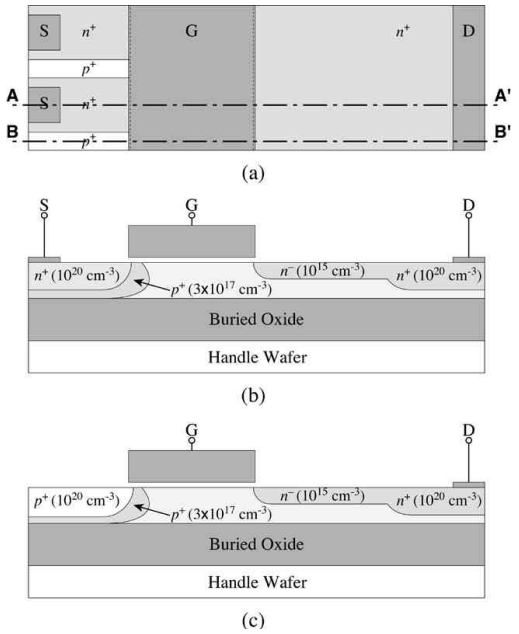

Fig. 1. Device structure showing (a) top view and cutlines *A*-*A*' and *B*-*B*' through (b) MOS and (c) body tie regions, respectively.

III. DC Characteristics

The DC characterization was performed using full Kelvin contacts to probe pads on the wafer surface. The Kelvin contacts ensured that cable parasitics were extracted from measured characteristics and that meter biasing was calibrated to on-wafer conditions.

Forward current-voltage operation is shown in Fig. 2 for gate biases to 4 V and drain bias up to 15 V. The measured response closely matches the design simulation except in the on-resistance of the triode regime which is degraded by the excessive resistance of the LDD. The increase in current observed in deep saturation at higher gate biases is due to the onset of bipolar conduction with holes injected into the base near the film-BOX interface. This is a thermally-enhanced mechanism. In electrothermal simulation, at drain biases of 15 V and gate bias of 4 V the film may develop hot spots of 100 °C over ambient conditions.

Measured and simulated device transconductance are plotted in Fig. 3 for a drain bias of 7.5 V, which is the intended drain bias of the RF amplifier. Again, the measured results are in good agreement with the design simulation except for the initial portion of the g_m response. This mismatch is caused by the slight disagreement between the designed threshold voltage (V_T = 1 V) and the measured value (1.25 V). All devices demonstrated good gain flatness for input voltages ranging from 2 to 4 V.

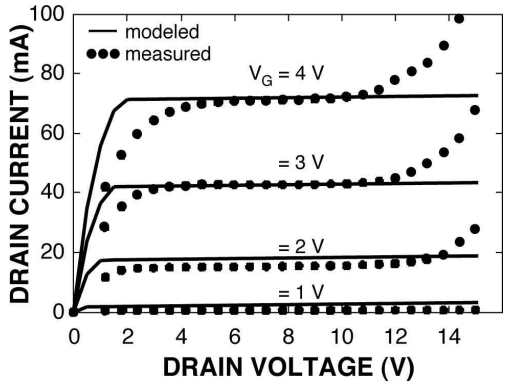

Fig. 2. Measured and modeled I-V response of the device.

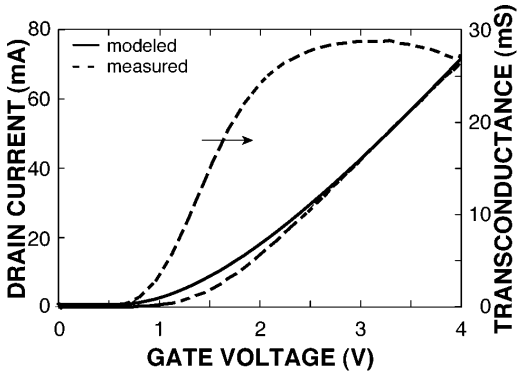

Fig. 3. Measured and modeled transconductance of the device (V_{DS} = 7.5 V).

IV. RF Characteristics

The RF characterization was performed using coplanar waveguide probes within an EMI- and light-free enclosure. Calibration to the probe pads was obtained using a ceramic impedance standard substrate (ISS) and the short-open-load-thru (SOLT) methodology.

Figure 4 shows the scattering parameters at a drain bias of 7.5 V and a drain current of 100 mA over the frequency range of 10 MHz to 3 GHz for an input signal of 0 dBm. The input reflection coefficient (s_{11}) matched the design simulation, except for a slight mismatch due to the gate resistance of the fabricated silicide. The difference of the simulated and actual gate resistance also degraded the measured forward transmission (s_{21}). Measured s_{21} becomes more uniform as the bias current is reduced to 5 mA, suggesting the mechanism for this disparity is g_m as a function of gate bias.

The measured output reflection coefficient (s_{22}) was significantly different than the design simulation, exhibiting much higher resistance. This is attributed to the increased resistance of the LDD region and its impact on the output impedance. The reverse transmission coefficient (s_{12}) of all devices was nearly equal.

The unity current gain frequency (f_T) was obtained for all devices by transforming the *S*-parameters to *H*-parameters and extrapolating the magnitude of h_{21} to 0 dB. These results are shown in Fig. 6. A peak f_T of 6.9 GHz was measured for a drain current of 25 mA. Using the power gain figure of merit of [9] the maximum oscillation frequency (f_{max}) was also extrapolated from its *S*-parameters to be 9.2 GHz.

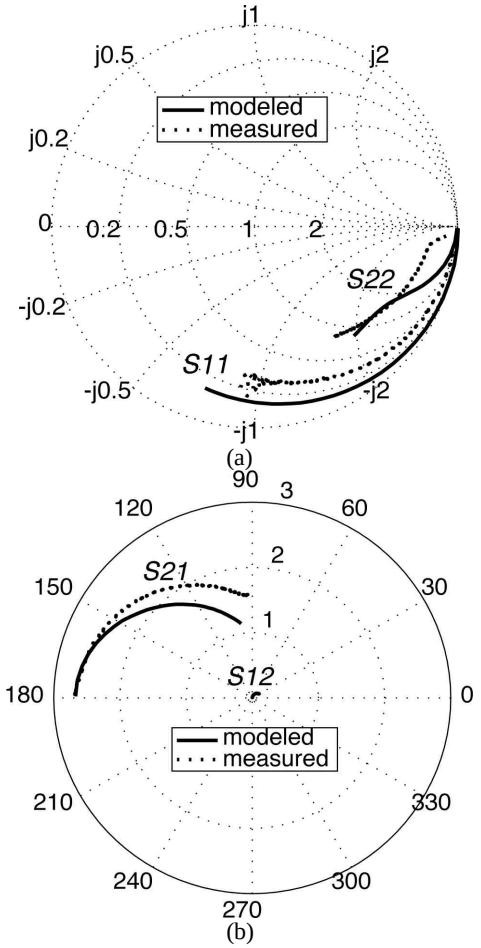

Fig. 5. Measured and modeled device (a) s_{11} and s_{22} and (b) s_{21} and s_{12} (V_{DS} = 7.5 V, V_{DG} = 2.35 V).

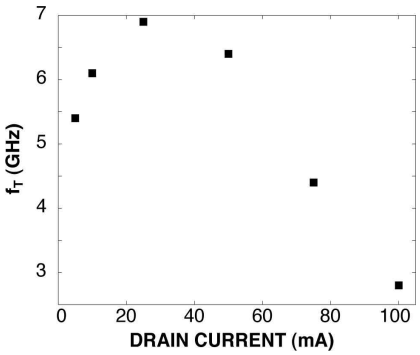

Fig. 6. Measured f_T versus drain current (V_{DS} = 7.5 V).

V. Model Parameter Extraction

Several simulation models have been proposed and demonstrated to produce an excellent match with measured characteristics in bulk RF LDMOSFETs, and the parameter extraction regime is well established [10]-[11]. Since these models were developed for bulk devices, they do not account for the effects of the buried dielectric. Also, these models include the effects of package parasitics. In this paper a reduced model was used to perform parameter extraction from on-wafer measurements. The equivalent circuit model is shown in Fig. 7.

From the DC measurements, the parameters of the three intrinsic active devices were extracted. A Spice level 3 model was used for the MOSFET. The MOSFET V_{t0} and k_p were obtained by fitting to three arbitrary points on the I_d-V_{ds} curve. Then, as per the parameter extraction regime of [12], the mobility and saturation velocity are derived from the g_m-V_{gs} plot. The extraction of [12] determines the JFET parameters from the transconductance compression that appears at higher gate biases. Since this device was designed to have minimal JFET saturation effects, reported techniques yield non-physical parameters for V_{t0j} and ß. Instead the V_{t0j} was determined empirically to be slightly less than the drain DC bias. The ß was then extracted using conventional analytical expressions. Finally, the diode resistance and the leakage path resistance were obtained by fitting the measured channel length modulation observed in the MOSFET saturation regime for larger gate biases (V_{gs} > 2 V). This is equivalent to the LAMBDA parameter of Spice level 1 and 2 MOSFET models.

The device input capacitance, C_{iss}, was obtained from direct on-wafer measurement; it matches with the device area and gate oxide thickness. The remaining capacitances and resistances were tuned empirically to fit the measured scattering parameters. A good match was obtained. The gate resistance, R_g, was used to match the real component of s_{11}. The diode capacitance (C_{j0}) and series resistance (R_s) were extracted by fitting s_{22} and s_{21}. Finally, the capacitance of the buried dielectric to the drain was fitted empirically using s_{22}, the drawn dimensions of the drain region, and the thickness of the buried dielectric.

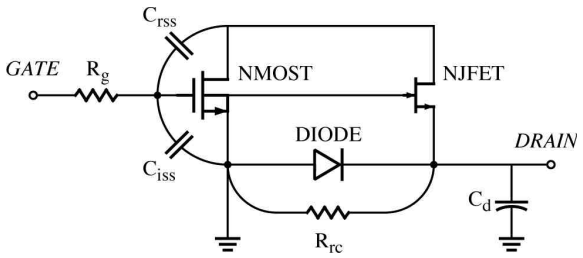

Fig. 7. Equivalent circuit model used for simulation.

TABLE I
EXTRACTED MODEL PARAMETERS

V_{t0} (V)	0.6
k_p (µS)	25
μ_0 (cm^2/V-sec)	300
v_{sat} (m/s)	6.8 x 10^4
V_{t0i} (V)	–7.4
ß (S)	6
C_{j0} (pF)	0.8
R_s (Ω)	250
C_{rss} (pF)	0.1
C_{iss} (pF)	1.0
C_d (pF)	0.4
R_g (Ω)	7
R_{rc} (Ω)	10

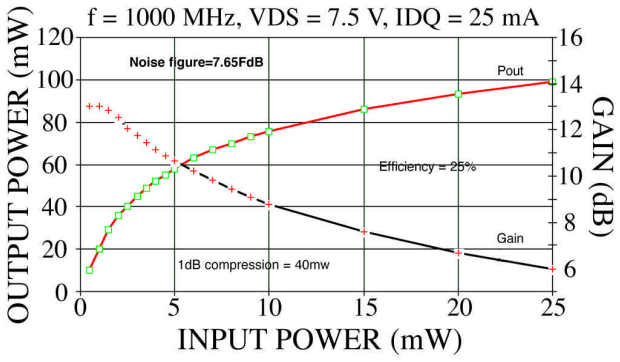

Fig. 8. Measured output power and power gain at 1-GHz operation. An efficiency of 25% was obtained.

VI. CLASS A RF POWER AMPLIFIER

Devices were packaged in a leaded RF package. Unlike bulk devices with a deep sinker implant, bond wires were required to connect the source bond pad to the carrier (similar to a packaged VDMOST). A 1-GHz narrow-band class A RF amplifier was built, and tuned input and output matching circuits were used to obtain maximum output power. It yielded an efficiency of 25% (identical to a similarly bulk LDMOSFET) with a maximum output of 0.115 W. A 1-dB compression of 40 mW of input power was observed and a noise figure of 7.65 dB was measured. Figure 8 shows the measured output power and gain. The presence of parasitic source inductance contributed to reducing gain to 13 dB. A large gain roll-off is caused by saturation of the transconductance, as shown in Fig. 3.

PAEs of MESFETs and HBTs at this power rating are 40-60%. Since Si LDMOSTs with PAE of 60% have been demonstrated we feel that with further optimization the SOI device will exceed 60%. In power gain, Si LDMOS lags its MESFET and HBT equivalents; however we expect a competitive gain of over 20 dB is possible with optimization. Improvement to the die wirebonding can reduce the impact of parasitic source inductance; similar refinement of the device structure can be performed to improve the flatness of the transconductance and reduce excessive gain roll-off.

VII. CONCLUSIONS

This paper reports the first results of 1-GHz SOI RF power LDMOSFETs. The performance achieved is promising and suggests that SOI LDMOSTs will be competitive with GaAs MESFET and SiGe HBT parts. The SOI substrate facilitates high-Q monolithic matching networks, and integration with peripheral digital or mixed-signal circuitry is simplified. These features make the SOI LDMOS a strong candidate for IPA development.

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